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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/705,050	11/02/2000	Masahiko Nakayama	P/1866-54	3890

7590 09/03/2003

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EXAMINER	
DO, CHAT C	
ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 09/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/705,050	NAKAYAMA, MASAHIKO	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/2/00; 4/9/01; 2/7/02; 1/31/03;4/15/03* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 November 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *1,4,6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. Figures 10-11 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Priority

2. Should applicant desire to obtain the benefit of foreign priority under 35 U.S.C. 119(a)-(d) prior to declaration of an interference, a translation of the foreign application should be submitted under 37 CFR 1.55 in reply to this action.

3. Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Claim Objections

4. Claims 1-2 are objected to because of the following informalities:

The applicant is advised to change the phrase "predetermined filter coefficient" in line 4 of claim 1 and in line 11 of claim 2 as "a predetermined filter coefficient".

In claim 2, there should be a right/closed parentheses such as "(n being natural number)".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 1, the limitation "the product output" lacks an antecedence basis. For examination purposes, the examiner considers this limitation as "a product output".

Re claim 2, the limitations "the feed-out" in line 7 and "the product outputs" in line 18 lack antecedence basis. For examination purposes, the examiner considers these limitations as "a feed-out" and "product outputs" respectively.

Re claim 6, the limitation "the shift clock frequency" lacks an antecedence basis. For examination purposes, the examiner considers this limitation as "a shift clock frequency".

Re claim 7, the limitation "the first and second n-bit shift registers" lack antecedence basis because these limitations have not mentioned in the preceded claim, claim 2. For examination purposes, the examiner disregards this limitation in the claim.

Thus, claims 3-5 and 8-9 are also rejected for being dependent on the rejected base claim 2.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Johannes et al. (U.S. 4,779,128).

Re claim 1, Johannes discloses in Figure 2 an FIR filter comprising a selection control means (20-24) for selecting input data (e.g. 30 or 35), and a multiplying means (51-59 odd number) for multiplying data selected (46-50) by the selection control means and a predetermined filter coefficient (52-60 even number), wherein the FIR filter output is derived from the product output of the multiplying means (output of 62).

9. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Hidemitsu (J.P. 411088119A).

Re claim 1, Hidemitsu discloses in Figure 1 an FIR filter comprising a selection control means (6-10) for selecting input data (either 1-5 or "0"), and a multiplying means (11-15) for multiplying data selected (inputs into 11-15 from 6-10) by the selection control means (6-10) and a predetermined filter coefficient (16-20), wherein the FIR filter output is derived from the product output of the multiplying means (output of 23 out).

Re claim 2, Hidemitsu discloses in Figure 1 an FIR filter (abstract) comprising: a selection control means (6-10), for selecting input data (either 1-5 or "0"), including a

first n-bit shift register (n being natural number) for progressively shifting the input data through the successive stage bits (n = 4), n switching means provided for the outputs of the n stage bits of the shift register (output of 6-10), respectively, for on-off controlling a feed-out of the output of theses stage bits (either on as real data from 1-5 or off as "0"), and a control means for on-off controlling the n switching means (22); and a multiplying means (11-15) for multiplying data selected by the selection control means and a predetermined filter coefficient (16-20), wherein the multiplying means provided for the outputs of the n stage bits of the shift register for multiplying outputs fed out from the corresponding stage bits under "on" control of the switching means by predetermined filter coefficients (16-20), respectively, and the FIR filter output being derived from the product outputs of the n multiplying circuits (output of 23 out).

Re claim 3, Hidemitsu further discloses in Figures 1 and 5 the control means (Figure 5) is constituted by a second n-bit shift register (60-62) for shifting a ramp-up/-down signal (51) through the successive bit stage under control of a shift clock for the first n-bit shift register; and the n switch means (6-10) are each an AND gate for receiving the outputs of the corresponding bit stage of the first and second n-bit shift registers as respective inputs (S1-S3).

Re claim 4, Hidemitsu further discloses in Figures 1 and 5 the control means (Figure 5) is a second n-bit shift register (60-62) for shifting a ram-up/-down signal (51) on the basis of the shift clock signal of the first n-bit shift register; and the n switching means (6-10) are n switches provided for the bit stages of the second n-bit sift register for

selectively feeding out the filter coefficient data and zero data on the basis of the outputs of the corresponding bit stages (S1-S3).

Re claim 5, Hidemitsu further discloses in Figures 1 and 5 the control means is a second n-bit shift register for shifting a ramp-up/-down signal through the successive bit stages under control of a shift clock signal for the first n-bit shift register, the outputs of the bit stages of the first n-bit shift register being reset on the basis of the outputs of the corresponding bit stage of the second n-bit shift register (Reset of 66).

10. Claims 1-2, 5-6, and 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Ikeda (U.S. 5,636,151).

Re claim 1, Ikeda discloses in Figure 3 an FIR filter comprising a selection control means (22) for selecting input data (20-X), and a multiplying means (24-X) for multiplying data selected (25-X) by the selection control means and a predetermined filter coefficient (Wx), wherein the FIR filter output is derived from the product output of the multiplying means (output of 26).

Re claim 2, Ikeda discloses in Figure 3 an FIR filter (abstract) comprising: a selection control means (33), for selecting input data (20-X), including a first n-bit shift register (21-X) for progressively shifting the input data through the successive stage bits (n = N), n switching means (22) provided for the outputs of the n stage bits of the shift register (output of 22), respectively, for on-off controlling a feed-out of the output of theses stage bits (col. 2 lines 57-63), and a control means for on-off controlling the n switching means (22); and a multiplying means (24-X) for multiplying data selected (25-

X) by the selection control means (33) and a predetermined filter coefficient (25-X), wherein the multiplying means provided for the outputs of the n stage bits of the shift register for multiplying outputs fed out from the corresponding stage bits under "on" control of the switching means by predetermined filter coefficients (W1-WK), respectively, and the FIR filter output being derived from the product outputs of the n multiplying circuits (output of 26).

Re claim 5, Ikeda further discloses in Figure 3 the control means (33) is a second n-bit shift register for shifting a ramp-up/-down signal (output of 27) through the successive bit stages under control of a shift clock signal for the first n-bit shift register, the outputs of the bit stages of the first n-bit shift register being reset (36) on the basis of the outputs of the corresponding bit stage of the second n-bit shift register.

Re claim 6, Ikeda further discloses in Figure 3 comprises a means for changing the shift clock frequency of the first n-bit shift registers (51).

Re claim 8, Ikeda further discloses in Figure 3 an adder circuit (26) for adding together the outputs of the n multiplying circuits (24-X), a ramp-up signal (output of 27) being fed to the first n-bit shift register, the ram-up data being derived from the sum output of the adder circuit (27).

Re claim 9, Ikeda further discloses in Figure 3 an adder circuit (26) for adding together the outputs of the n multiplying circuits (24-X), a ramp-down signal (output of 27) being fed to the first n-bit shift register, the ram-down data being derived from the sum output of the adder circuit (27).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 6,058,407 to Kim discloses a FIR filter with non-symmetric frequency response characteristics.

b. U.S. Patent No. 4,872,184 to Yamaguchi et al. disclose a digital automatic line equalizer with means for controlling tap gains of transversal filter based on mean power of output from the filter.

c. U.S. Patent No. 5,422,606 to Tanaka discloses an automatic equalizer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Chat C. Do
Examiner
Art Unit 2124

JOHN CHAVIS
PATENT EXAMINER
ART UNIT 2124